

METHOD OF DRIVING SURFACE DISCHARGE PLASMA DISPLAY PANEL

Technical Field

5 The present invention relates to a method of driving a surface discharge plasma display panel, and more particularly, to a method for driving a three-electrode surface-discharge alternating-current plasma display panel(AC PDP).

Background Art

10 FIG. 1 shows an electrode pattern of a conventional surface discharge plasma display panel. FIG. 2 is a schematic sectional view of a pixel of FIG. 1. Referring to FIGS. 1 and 2, the conventional surface discharge plasma display panel includes address electrodes A1, A2, A3, ..., Am, a first dielectric 21, a luminescent material 22, scan electrodes Y1, Y2, ..., Yn-1, Yn, 231, 232, common electrodes X, 241, 242, a second dielectric 25, and a protective layer 26. Each of the scan electrodes Y1, Y2, ..., Yn-1, Yn, includes an indium tin oxide (ITO) scan electrode 231 and a bus scan electrode 232. In the same manner, each of the common electrodes X, 241, 242 includes a common ITO electrode 241 and a common bus electrode 242. Gas for forming plasma is sealed between the protective layer 26 and a first dielectric 21.

20 a The address electrodes A1, A2, A3, ..., Am are coated on a lower substrate (not shown) of a first substrate in a predetermined pattern. The first dielectric 21 is coated on the address electrodes A1, A2, A3, ..., Am. The luminescent material 22 is coated on the first dielectric 21 in a predetermined pattern. Depending on circumstances, without forming the first dielectric 21, the luminescent material 22 may be coated on the address electrodes A1, A2, A3, ..., Am, in a predetermined pattern. The scan electrodes Y1, Y2, ..., Yn-1, Yn, 231, 242 and the common electrodes X, 241, 242 are formed on an upper substrate (not shown) of a second substrate, such that they intersect with the address electrodes A1, A2, A3, ..., Am. 25 The respective intersections each define a corresponding pixel. The second dielectric 25 is coated on the scan electrodes Y1, Y2, ..., Yn-1, Yn, 231, 232 and the common electrodes X, 241, 242. The protective layer 26 for protecting the 30

panel from a strong electrical field is coated on the second dielectric 25.

In the prior art driving method of a surface discharge plasma display panel, a relatively high voltage is applied between the scan electrodes Y1, Y2, ..., Yn-1, Yn, 231, 232 and the common electrodes X, 241, 242 to accumulate wall charges in the respective pixel by a surface discharge, and the wall-charges accumulated by the surface discharge are removed, in a resetting step. The conventional driving method is disclosed in U.S. Patent No. 5,446,344.

FIG. 3 is for illustrating a conventional driving method of a surface discharge plasma display panel.

In a first reset interval (a-b), a pulse of voltage V_{aw} , a pulse of voltage V_s+V_w , and 0 V are applied to the address electrodes Am, the common electrodes X, and the scan electrodes Y1, Y2, ..., Yn, respectively. Here, the voltage V_s+V_w obtained by adding the voltage V_w to the scan voltage V_s is higher than the voltage V_{aw} . Accordingly, a relatively high voltage V_s+V_w is applied between the common electrodes X and the scan electrodes Y1, Y2, ..., Yn, so that a surface discharge occurs between the common electrodes X and the scan electrodes Y1, Y2, ..., Yn ('a' of FIG. 3). And then, positive(+) wall-charges are accumulated in the positive layer 26 of FIG. 2 under each of the scan electrodes 231, 232 of FIG. 2, and negative(-) wall-charges are accumulated in the positive layer 26 under the common electrodes 241, 242 of FIG. 2.

The voltage of the wall-charges accumulated during the first reset interval (a-b) is a re-dischargeable voltage. In a second reset interval (b-c), 0 V is applied to the address electrodes Am, the common electrodes X, and the scan electrodes Y1, Y2, ..., Yn. Accordingly, due to the wall-charges accumulated during the first reset interval (a-b), a surface discharge occurs between the common electrodes X and the scan electrodes Y1, Y2, ..., Yn. And then, the wall-charges of all pixels are removed.

In an address step, in a state in which a pulse of voltage V_{ax} is applied to the common electrodes X, scan pulses of a voltage $-V_y$ are sequentially applied to each of the scan electrodes Y1, Y2, ..., Yn. When the scan pulse is not applied, a negative voltage $-V_{sc}$ which is a level lower than the voltage $-V_y$ of the scan pulse is applied. When a pulse of the address voltage V_a is applied to an address

electrode Am selected while the scan pulse is applied to a scan electrode Y1, Y2, ..., Yn, for example, during interval (c-d) for the scan electrode Y1, a facing discharge is performed in a corresponding pixel. This is because a voltage for facing discharge $V_a + V_y$ is applied between the corresponding scan electrode Y1, Y2, ..., or Yn and the selected address electrode Am. At this time, when a negative voltage $-V_{sc}$ which is lower than the voltage $-V_y$ of the scan pulse is applied, the facing discharge stops. And then, ^{positive(+)} wall-charges are ^{then} accumulated under the scan electrodes 231, 232 of the selected pixel.

In a first sustaining discharge interval (g-h), a pulse of the voltage $V_s/2$ which is $\frac{1}{2}$ the scan voltage V_s , 0V, and a pulse of the sustaining discharge voltage V_s , are applied to the address electrodes Am, the common electrode X, and the scan electrodes Y1, Y2, ..., Yn, respectively. That is, in a state in which positive(+) wall-charges are accumulated under the scan electrode Y1, Y2, ..., or Yn of the selected pixel, when a relatively high negative-voltage is applied between the scan electrodes Y1, Y2, ..., Yn and the common electrodes X, a surface discharge occurs in the selected pixel. When the surface discharge is performed in the selected pixel, plasma is formed in a gas layer of a corresponding region, and a luminescent material 22 of FIG. 2 is excited by an UV-ray to emit light.

In a second sustaining discharge interval (i-j), a pulse of the voltage $V_s/2$ which is $\frac{1}{2}$ the scan voltage V_s , ^{and} a pulse of the sustaining discharge voltage V_s , and 0V, are applied to the address electrodes Am, the common electrodes X, and the scan electrodes Y1, Y2, ..., Yn, respectively. That is, in a state in which wall-charges are accumulated, when a relatively high negative voltage is applied between the scan electrodes Y1, Y2, ..., Yn and the common electrodes X, a surface discharge occurs in a selected pixel. And then, ^{positive(+)} wall-charges are ^{then} accumulated under the scan electrodes 231, 232 of the selected pixel, and negative(-) wall-charges are accumulated under the common electrodes 241, 242. When the surface discharge is performed in the selected pixel, plasma is formed in a gas layer of a corresponding region, and a luminescent material 22 is excited by a UV-ray to emit light. The operations of the first and second sustained discharge intervals are repeated during the sustaining discharge period, to thereby

maintain the emission of light at the selected pixel.

In the conventional driving method, in the resetting step (interval a-c of FIG. 3), a pulse of a relatively high voltage V_s+V_w is applied between the common electrodes X and the scan electrodes Y1, Y2, ..., Yn, so that a surface discharge occurs. Accordingly, the light of relatively high brightness is emitted from the unselected pixels, to thereby decrease the contrast of a display screen.

Disclosure of Invention

It is an object of the present invention to provide a driving method of a surface discharge plasma display panel for emitting the light of relatively low brightness from the pixels unselected in each sub-field.

To accomplish the above object of the present invention, a driving method of a surface discharge plasma display panel is adopted to a surface discharge plasma display panel having a first substrate and a second substrate space apart and facing each other, and common electrodes, scan electrodes, and address electrodes arranged between said first and second substrates, said common electrodes being arranged in parallel with said scan electrodes, said address electrodes being arranged orthogonal to said common electrodes and said scan electrodes to form respective intersections which each define a corresponding pixel.

The driving method of a surface discharge plasma display panel comprises a reset step, an address step, and a sustaining discharging step. In the reset step, a first voltage is applied between the scan electrodes and the address electrodes to accumulate wall charges in the respective pixel by a facing discharge, and the wall-charges accumulated by the facing discharge are removed. In the address step, a second voltage is applied between a corresponding scan electrodes and selected address electrodes so that a facing discharge occurs, to form wall-charges in the selected pixels. In the sustaining discharge step, a third alternating-current voltage is applied between the scan electrodes and the common electrodes so that a surface discharge occurs in the selected pixels.

In the reset step of the present invention, the wall charges to be removed are accumulated by the facing discharge. Accordingly, the light of relatively low brightness is emitted from the pixels unselected in each sub-field.

Preferably, the reset step includes a first, a second and a third reset step.

5 In the first reset step, a fourth voltage is applied between the scan electrodes and the common electrodes, and thereby remove remnant wall-charges from a previous sub-field, said fourth voltage has an opposite polarity to a voltage applied last in the sustained discharging step. In the second reset step, said first voltage is applied between the scan electrodes and the address electrodes, and thereby
10 cause the facing discharge. In the third reset step, a fifth voltage is applied between the scan electrodes and the address electrodes, and thereby remove wall-charges accumulated by the facing discharge, said fifth voltage has an opposite polarity to said first voltage and lower than said first voltage. Also, the third reset step is shorter than the first and second reset steps. And, the third
15 reset step is repeated.

Brief Description of Drawings

The above objects and advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with
20 reference to the attached drawings in which:

a FIG. 1 is a diagram ^{of} showing a typical electrode pattern of a surface discharge plasma display panel;

FIG. 2 is a schematic sectional view of a pixel of the pattern of FIG. 1;

a FIG. 3 is a diagram ^{of} showing voltage waveforms applied to electrodes according to a plasma display panel driving method based on a prior art.

a FIG. 4 is a diagram ^{of} showing voltage waveforms applied to electrodes according to a plasma display panel driving method based on an embodiment of the present invention.

a FIG. 5 is a diagram ^{of} showing the state of a selected pixel during a last sustaining discharge interval (O-P) of FIG. 4;

a FIG. 6A is a diagram ^{of} showing the state of a unit pixel in a first reset interval (A-B) of FIG. 4;

FIG. 6B is a diagram ^{of} showing the state of a unit pixel during a second reset interval (C-D) of FIG. 4; and

FIG. 6C is a diagram ^{of} showing the state of a unit pixel in a third reset interval (E-F) of FIG. 4.

FIG. 7 is a diagram ^{of} showing the state of a pixel selected during an address interval (G-K) of FIG. 4.

FIG. 8A is a diagram ^{of} showing the state of a pixel selected during a first sustaining discharge interval (K-L) of FIG. 4

FIG. 8B is a diagram ^{of} showing the state of a pixel selected during a second sustaining discharge interval (M-N) of FIG. 4

FIG. 9 is a diagram ^{of} showing voltage waveforms applied to electrodes according to a plasma display panel driving method based on the other embodiment of the present invention.

Best Mode for Carrying Out the Invention

FIG. 4 ^{is an illustration of} shows the voltage waveforms applied to electrodes according to a plasma display panel driving method based on an embodiment of the present invention. Referring to FIG. 4; In the reset interval (A-G), a first voltage V_w is applied between the scan electrodes Y_1, Y_2, \dots, Y_n and the address electrodes A_m to accumulate wall charges in the respective pixel by a facing discharge, and the wall-charges accumulated by the facing discharge are removed. In the address interval (G-K), a second voltage $V_a + V_k + V_y$ is applied between a corresponding scan electrodes Y_1, Y_2, \dots, Y_n and selected address electrodes A_m so that a facing discharge occurs, to form wall-charges in the selected pixels. In the sustaining discharge interval (K-Q), a third alternating-current voltage $V_s + V_k$ is applied between the scan electrodes Y_1, Y_2, \dots, Y_n and the common electrodes X so that a surface discharge occurs in the selected pixels.

In the reset interval (A-G) of this embodiment, the wall charges to be removed are accumulated by the facing discharge. Accordingly, the light of relatively low brightness is emitted from the pixels unselected in each sub-field. Also, there are residual wall charges on the address electrodes A_m in the reset interval (A-G), and thereby the second voltage $V_a + V_k + V_y$ applied in the address

interval (G-K) can be lowered.

Three steps are sequentially performed in the reset interval (A-G). In the first reset step (interval A-B), a fourth voltage V_s+V_k is applied between the scan electrodes Y1, Y2, ..., Yn and the common electrodes X, and thereby remove
5 remnant wall-charges from a previous sub-field, the fourth voltage V_s+V_k has an opposite polarity to a voltage applied last in the sustained discharging interval (K-Q). In the second reset step (interval C-D), the first voltage V_w is applied between the scan electrodes Y1, Y2, ..., Yn and the address electrodes Am, and thereby cause the facing discharge. In the third reset step (interval E-F), a fifth voltage V_k
10 is applied between the scan electrodes Y1, Y2, ..., Yn and the address electrodes Am, and thereby remove wall-charges accumulated by the facing discharge, the fifth voltage V_k has an opposite polarity to the first voltage V_w and lower than the first voltage V_w . The third reset interval (E-F) is shorter than the first (A-B) and second (C-D) reset intervals. Also, the third reset step (interval E-F) is repeated.

A driving method of FIG. 4 is adopted for the case that 0V, a negative(-) voltage $-V_k$ of a relatively high level, for example, -140V, and a positive(+) voltage V_s of a relatively low level, for example, 40V, are applied to address electrodes Am, common electrodes X, and scan electrodes Y1, Y2, ..., Yn, respectively.
15 Here, negative(-) wall-charges are accumulated under the scan electrodes 231, 232 of a selected pixel, and positive(+) wall-charges are accumulated under the common electrodes 241, 242, as shown in FIG. 5. Reference numerals of FIG. 5 which are the same as those of FIG. 2 indicate identical elements. Meanwhile, wall-charges are not accumulated in unselected pixel regions.

In the first reset interval (A-B), 0V, a pulse of the positive(+) voltage V_s , and
25 a pulse of the negative(-) voltage $-V_k$ are applied to the address electrodes Am, the common electrodes X, and the scan electrodes Y1, Y2, ..., Yn, respectively. That is, in a state in which the voltage of the address electrodes Am is maintained at 0V, a voltage applied between the common electrodes X and the scan electrodes Y1, Y2, ..., Yn is a negative voltage V_s+V_k of the voltage $-(V_s+V_k)$ of a
30 final sustaining discharge interval of a previous sub-field. Accordingly, the wall-charges in the pixels selected in a previous sub-field are removed. Also, as shown in FIG. 6A, positive(+) wall-charges are accumulated in a protective layer

26 under each of the scan electrodes 231, 232 of the pixel selected in the previous sub-field, and negative(-) wall-charges are accumulated in the protective layer 26 under the common electrodes 241, 242. Reference numerals of FIG. 6A which are the same as those of FIG. 2 indicate identical elements. Meanwhile, wall-charges are not accumulated in a pixel region not selected from the previous sub-field.

In the second reset interval (C-D), 0V, ~~a~~ a pulse of the positive(+) voltage Vs, and ~~a~~ a pulse of the positive(+) voltage Vw for facing discharge, for example, 180 V, are applied to the address electrodes Am, the common electrodes X, and the scan electrodes Y1, Y2, ..., Yn, respectively. That is, the relatively high voltage Vw is applied between the address electrodes Am and the scan electrodes Y1, Y2, ..., Yn. Accordingly, a facing discharge occurs between the address electrodes Am of pixels where wall-charges are accumulated in the first reset interval (A-B), that is, the pixels selected from the previous sub-field, and the scan electrodes Y1, Y2, ..., Yn. Meanwhile, a facing discharge does not occur between the address electrodes Am of pixels where wall-charges are not accumulated in the first reset interval (A-B), that is, the pixels not selected from the previous sub-field, and the scan electrodes Y1, Y2, ..., Yn. As shown in FIG. 6B, negative(-) wall-charges are accumulated in the protective layer 26 under the scan electrodes 231, 232 of each pixel selected from the previous sub-field, and the positive(+) wall-charges are accumulated in a luminescent material 22 of the address electrodes Am. Here, positive(+) wall-charges are accumulated in the protective layer 26 under the common electrodes 241, 242. Reference numerals of FIG. 6B which are the same as those of FIG. 2 indicate identical elements. Meanwhile, wall-charges are not accumulated in a pixel region not selected from the previous sub-field.

In the third reset interval (E-F), 0 V is applied to the address electrodes Am and the common electrodes X, and a pulse of the negative(-) voltage -Vk is applied to the scan electrodes Y1, Y2, ..., Yn. The operation of the third reset interval is performed relatively quickly, so that the pulse width of the negative(-) voltage -Vk applied to the scan electrodes Y1, Y2, ..., Yn, is relatively short. As shown in FIG. 4, the operation of the third reset interval (E-F) is sequentially

performed again. Accordingly, as shown in FIG. 6C, the wall-charges of the pixels selected from the previous sub-field are removed. Nevertheless, there are residual wall charges on the address electrodes A_m in the reset interval (A-G), and thereby the second voltage $V_a + V_k + V_y$ applied in the address interval (G-K) can be lowered. Reference numerals of FIG. 6C which are the same as those of FIG. 2 indicate identical elements.

a
a
Then, ^{IN} in the address period (G-K), in a state in which a pulse of the positive(+) voltage V_s is ^{then} applied to the common electrodes X, scan pulses of the negative voltage $-V_k - V_y$ higher than the negative(-) voltage $-V_k$, for example, -180V, are sequentially applied to each of the scan electrodes Y_1, Y_2, \dots, Y_n . When the scan pulse is not applied, a negative voltage $-V_p$ lower than the negative(-) voltage $-V_k$ is applied. When an address voltage V_a , for example, 80V, is applied to an address electrode A_m selected while the scan pulse is applied to one of the corresponding scan electrodes Y_1, Y_2, \dots, Y_n , for example, G-H interval for the scan electrode Y_1 , facing discharge occurs in a corresponding pixel. This is because a voltage for facing discharge $V_k + V_y + V_a$, for example, 260V, is applied between the corresponding scan electrode Y_1, Y_2, \dots, Y_n and a selected address electrode A_m . Here, the negative voltage $-V_k - V_y$ higher than the negative voltage $-V_k$ is applied to each of the scan electrodes Y_1, Y_2, \dots, Y_n , to thereby relatively lower the address voltage V_a . When the negative voltage $-V_p$ is applied when the facing discharge occurs, the facing discharge ceases. As shown in FIG. 7, positive(+) wall-charges are accumulated under the scan electrodes 231, 232 of a selected pixel. Reference numerals of FIG. 7 which are the same as those of FIG. 2 indicate identical elements.

a
In the first sustaining discharge interval (K-L), 0 V is applied to the address electrodes A_m , a pulse of the negative(-) voltage $-V_k$ is applied to the common electrodes X, and a pulse of the positive(+) voltage V_s is applied to scan electrodes Y_1, Y_2, \dots, Y_n . And thereby, surface discharges occur in the selected pixels. As shown in FIG. 8A, negative(-) wall-charges are accumulated under scan electrodes 231, 232 of the selected pixel, and positive(+) wall-charges are accumulated under the common electrodes 241, 242. Reference numerals of FIG. 8A which are the same as those of FIG. 2 indicate identical elements. When a

surface discharge occurs in the selected pixel, plasma is formed in a gas layer of a corresponding region, and a luminescent material 22 is excited by a UV-ray, to emit light.

In the second sustaining discharge interval, 0 V is applied to the address electrodes Am, a pulse of the positive(+) voltage Vs is applied to the common electrodes X, and a negative(-) voltage -Vk is applied to the scan electrodes Y1, Y2, ..., Yn. And thereby, surface discharges occur in the selected pixels. As shown in FIG. 8B, positive(+) wall-charges are accumulated under the scan electrodes 231, 232 of the selected pixel, and negative(-) wall-charges are accumulated under the common electrodes 241, 242. Reference numerals of FIG. 8B which are the same as those of FIG. 2 indicate identical elements. when a surface discharge occurs in the selected pixel, plasma is formed in a gas layer of a corresponding region, and the luminescent material 22 is excited by a UV-ray, to thereby emit light. The operations of the first and second sustaining discharge steps (interval K-N) are repeated during a predetermined sustaining discharge interval (K-Q), to maintain illumination of the selected pixel.

FIG. 9 shows voltage waveforms applied to electrodes according to a plasma display panel driving method based on the other embodiment of the present invention. Comparing FIG. 9 to FIG. 4, the voltage waveform applied to the common electrodes X is changed in the reset interval (A-G). The operation in the address and sustaining discharge interval (G-Q) is same as that described above. So, referring to FIG. 9, the operation in only the reset interval (A-G) will be explained.

In the first reset interval (A-B), 0 V is applied to the Address electrodes Am and the common electrodes X, and a pulse of the negative(-) voltage -Vk are applied to the scan electrodes Y1, Y2, ..., Yn. Accordingly, the wall-charges in the pixels selected in a previous sub-field are removed. Also, as shown in FIG. 6A, positive(+) wall-charges are accumulated in a protective layer 26 under each of the scan electrodes 231, 232 of the pixel selected in the previous sub-field, and negative(-) wall-charges are accumulated in the protective layer 26 under the common electrodes 241, 242. Meanwhile, wall-charges are not accumulated in a pixel region not selected from the previous sub-field.

In an additional reset interval (B-C), 0 V, a pulse of the positive(+) voltage +Vs, and a pulse of the negative(-) voltage -Vk are applied to the address electrodes Am, the scan electrodes Y1, Y2, ..., Yn, and the common electrodes X, respectively. Accordingly, the wall-charges accumulated in the first reset interval (A-B) are removed.

In the second reset interval (C-D), 0V is applied to the address electrodes Am and the common electrodes X, and a pulse of the positive(+) voltage Vw for facing discharge, for example, 180 V, are applied to the scan electrodes Y1, Y2, ..., Yn. Accordingly, a facing discharge occurs between the address electrodes Am of pixels where wall-charges are accumulated in the first reset interval (A-B), that is, the pixels selected from the previous sub-field, and the scan electrodes Y1, Y2, ..., Yn. Meanwhile, a facing discharge does not occur between the address electrodes Am of pixels where wall-charges are not accumulated in the first reset interval (A-B), that is, the pixels not selected from the previous sub-field, and the scan electrodes Y1, Y2, ..., Yn. As shown in FIG. 6B, negative(-) wall-charges are accumulated in the protective layer 26 under the scan electrodes 231, 232 of each pixel selected from the previous sub-field, and the positive(+) wall-charges are accumulated in a luminescent material 22 of the address electrodes Am. Here, positive(+) wall-charges are accumulated in the protective layer 26 under the common electrodes 241, 242. Meanwhile, wall-charges are not accumulated in a pixel region not selected from the previous sub-field.

In the third reset interval (E-F), 0 V is applied to the address electrodes Am and the common electrodes X, and a pulse of the negative(-) voltage -Vk is applied to the scan electrodes Y1, Y2, ..., Yn. The operation of the third reset interval is performed relatively quickly, so that the pulse width of the negative(-) voltage -Vk applied to the scan electrodes Y1, Y2, ..., Yn, is relatively short. The operation of the third reset interval (E-F) is sequentially performed again. Accordingly, as shown in FIG. 6C, the wall-charges of the pixels selected from the previous sub-field are removed. Also, the additional reset interval (B-C) is repeated after the the third reset interval (E-F), and thereby, most of the remnant wall charges can be removed. Nevertheless, there are residual wall charges on the address electrodes Am in the reset interval (A-G), and thereby the second

voltage $V_a+V_k+V_y$ applied in the address interval (G-K) can be lowered.

Industrial Applicability

As described above, according to a driving method of a surface discharge type alternating current plasma display panel of the present invention, the wall charges to be removed are accumulated by the facing discharge in the reset step. Accordingly, the light of relatively low brightness is emitted from the pixels unselected in each sub-field, to thereby increase the contrast of the display screen. Also, there are residual wall charges on only the address electrodes after the reset step, and thereby the voltage applied in the address interval can be lowered.

The present invention is not limited to the illustrated embodiment and many changes and modifications can be made within the scope of the invention by a person skilled in the art.